AFFILIATED INSTITUTIONS

ANNA UNIVERSITY, CHENNAI

REGULATIONS – 2009

M.E. EMBEDDED SYSTEMS

II- IV SEMESTERS(FULL TIME) CURRICULUM AND SYLLABUS

SEMESTER II

COURSE CODE	COURSE TITLE	L	T	P	C
THEORY					
SY9321	Real Time Operating System	3	1	0	4
SY9322	Embedded Control Systems	3	0	0	3
SY9323	Software Technology for Embedded Systems	3	0	0	3
ET 9223	Embedded Networking	3	1	0	4
	Elective II	3	0	0	3
	Elective III	3	0	0	3
PRACTICAL					
SY9324	Embedded System Lab II	0	0	3	2
	TOTAL CREDITS	**18**	**2**	**3**	**22**

SEMESTER III

COURSE CODE	COURSE TITLE	L	T	P	C
THEORY					
	Elective IV	3	0	0	3
	Elective V	3	0	0	3
	Elective VI	3	0	0	3
PRACTICAL					
SY9331	Project Work (Phase I)	0	0	12	6
	TOTAL CREDITS	**9**	**0**	**12**	**15**

SEMESTER IV

COURSE CODE	COURSE TITLE	L	T	P	C
Practical					
SY9341	Project Work (Phase II)	0	0	24	12
	TOTAL CREDITS	**0**	**0**	**24**	**12**

TOTAL CREDITS TO BE EARNED FOR THE AWARD OF THE DEGREE 22+22+15+12= 71

LIST OF ELECTIVES
For SEMESTER II (ELECTIVE – II AND ELECTIVE – III)

Course Code	Course Title	L	T	P	C
SY9351	Data Communication & Networks	3	0	0	3
SY9352	Digital Image Processing	3	0	0	3
SY9353	ASIC Design	3	0	0	3
SY9354	Advanced Embedded Systems	3	0	0	3
SY9355	Computer Architecture	3	0	0	3
SY9356	Multimedia Systems	3	0	0	3
SY9357	Operating Systems	3	0	0	3
SY9358	VHDL	3	0	0	3

For SEMESTER III (ELECTIVE – IV, ELECTIVE – V AND ELECTIVE – VI)

Course Code	Course Title	L	T	P	C
SY9359	Advanced Microprocessors and Microcontrollers Design	3	0	0	3
SY9360	DSP Integrated Circuits	3	0	0	3
SY9361	Embedded Analog Interfacing	3	0	0	3
SY9362	Embedded Automotive Networking with CAN	3	0	0	3
SY9363	Real Time Systems	3	0	0	3
SY9364	Real Time Embedded Operating Systems	3	0	0	3
SY9365	VLSI Architecture and Design Methodologies	3	0	0	3
SY9366	Embedded System Design using ARM Processor	3	0	0	3
	Special Elective	3	0	0	3

SY9321 REAL TIME OPERATING SYSTEMS L T P C
3 1 0 4

UNIT - I REVIEW OF OPERATING SYSTEMS 9

Basic Principles – System Calls – Files – Processes – Design and Implementation of processes – Communication between processes – Operating System structures.

UNIT - II DISTRIBUTED OPERATING SYSTEMS 9

Topology – Network types – Communication – RPC – Client server model – Distributed file system – Design strategies.

UNIT - III REAL TIME MODELS AND LANGUAGES 9

Event Based – Process Based and Graph based Models – Petrinet Models – Real Time Languages – RTOS Tasks – RT scheduling - Interrupt processing – Synchronization – Control Blocks – Memory Requirements.

UNIT - IV REAL TIME KERNEL 9

Principles – Design issues – Polled Loop Systems – RTOS Porting to a Target – Comparison and study of various RTOS like QNX – VX works – PSOS – C Executive – Case studies.

UNIT - V RTOS APPLICATION DOMAINS 9

RTOS for Image Processing – Embedded RTOS for voice over IP – RTOS for fault Tolerant Applications – RTOS for Control Systems.

TOTAL: 45 PERIODS

REFERENCES:

1. Herma K., “Real Time Systems – Design for distributed Embedded Applications”, Kluwer Academic, 1997.
2. Charles Crowley, “Operating Systems-A Design Oriented approach” McGraw Hill 1997.
3. C.M. Krishna, Kang, G.Shin, “Real Time Systems”, McGraw Hill, 1997.
4. Raymond J.A.Bhur, Donald L.Bailey, “An Introduction to Real Time Systems”, PHI 1999.

SY9322 EMBEDDED CONTROL SYSTEMS L T P C
3 0 0 3

UNIT – I INTRODUCTION 6

Controlling the hardware with software – Data lines – Address lines - Ports – Schematic representation – Bit masking – Programmable peripheral interface – Switch input detection – 74 LS 244

UNIT – II INPUT-OUTPUT DEVICES 8

Keyboard basics – Keyboard scanning algorithm – Multiplexed LED displays – Character LCD modules – LCD module display – Configuration – Time-of-day clock – Timer manager - Interrupts - Interrupt service routines – IRQ - ISR – Interrupt vector or dispatch table multiple-point - Interrupt-driven pulse width modulation.

UNIT – III D/A AND A/D CONVERSION 12

R 2R ladder - Resistor network analysis - Port offsets - Triangle waves analog vs. digital values - ADC0809 – Auto port detect - Recording and playing back voice - Capturing analog information in the timer interrupt service routine - Automatic, multiple channel analog to digital data acquisition.

UNIT – IV ASYNCHRONOUS SERIAL COMMUNICATION 9

Asynchronous serial communication – RS-232 – RS-485 – Sending and receiving data – Serial ports on PC – Low-level PC serial I/O module - Buffered serial I/O.

UNIT - V CASE STUDIES: EMBEDDED C PROGRAMMING 10

Multiple closure problems – Basic outputs with PPI – Controlling motors – Bidirectional control of motors – H bridge – Telephonic systems – Stepper control – Inventory control systems.

TOTAL: 45 PERIODS

REFERENCES:

1. Jean J. Labrosse, “Embedded Systems Building Blocks: Complete and Ready- To-Use Modules in C”The publisher, Paul Temme, 1999.
2. Ball S.R., ‘Embedded microprocessor Systems – Real World Design’, Prentice Hall, 1996.
3. Herma K, “Real Time Systems – Design for distributed Embedded Applications”, Kluwer Academic, 1997.
4. Daniel W. Lewis, “Fundamentals of Embedded Software where C and Assembly meet”, PHI, 2002.

SY9323 SOFTWARE TECHNOLOGY FOR EMBEDDED SYSTEMS **L T P C 3 0 0 3**

UNIT – I BASIC CONCEPTS IN OBJECT-ORIENTED METHODOLOGY 9

Benefits of object-oriented methodology. Class & Objects - Definitions - How to determine the object and classes, where to look, what to look for, what to consider and challenge, examples. Identifying structures: Definitions - generalization - specialization, whole-part structures, examples. Definitions - examples. Defining attributes - Definitions - How to determine the attributes, Instance connections, examples. Defining services, message connections, specifying services, final class and object specification examples.

UNIT – II OBJECT ORIENTED ANALYSIS 9

Connecting the Object Model with the Use Case Model - Key strategies for Object – Identification – Underline the Noun strategy. Identify the Casual Objects – Identify Services (Passive Contributors) – Identify Real-World Items – Identify Physical Devices – Identify Key Concepts – Identify Transactions – Identify persistent information – Identify visual elements – Identify control elements – Apply scenarios

UNIT - III OBJECT ORIENTED SYSTEMS DEVELOPMENT 9

Introduction to object oriented systems development – Procedure oriented paradigms – Procedure oriented development tools – Object Oriented paradigm – Object Oriented notations and graphs – Steps in Object Oriented Analysis – Steps in Object Oriented analysis – Steps in Object Oriented design – Prototyping paradigm - Approach to Object Oriented Design – The programming problem – The CRC modeling team – Constructing the CRC cards – Use Cases – Class relationships – Class Diagrams

UNIT – IV UNIFIED MODELING LANGUAGE 9

Object state behaviour – UML state charts – Role of scenarios in the definition of behaviour – Timing diagrams – Sequence diagrams – Event hierarchies – Types and strategies of operations – Architectural design in UML concurrency design – Representing tasks – System task diagram – Concurrent state diagrams – Threads – Mechanistic design – Simple patterns.

UNIT – V CASE STUDIES 9

Multi threaded applications – Assembling embedded applications – Polled waiting loop and interrupt driven I/O – Preemptive kernels and shared resources – System timer – Scheduling – Client server computing

TOTAL: 45 PERIODS

REFERENCES:

1. Peter Coad and Edward Yourdon, “Object Oriented Analysis”, PH, 2nd Edn.,1991
2. Peter Coad and Edward Yourdon, “Object Oriented Design”, PH, 1991.
3. Bruce Powel Douglas, “Real-Time UML: Developing Efficient Objects for Embedded Systems” 2nd Edition, Addison – Wesley, 1999.
4. Hassan Gomma, “Designing concurrent, distributed, and Real-Time applications with UML”
5. Robert Lafore, “Object Oriented Programming in C++”, Galgotia Publications Pvt. Ltd., 3rd Edition, 2001

ET9223	EMBEDDED NETWORKING	L T P C
		3 1 0 4

UNIT - I EMBEDDED COMMUNICATION PROTOCOLS 8

Embedded Networking:Introduction–Serial / ParallelCommunication–Serial communication protocols -RS232 standard – RS485 – Synchronous Serial Protocols - Serial Peripheral Interface (SPI) – Inter Integrated Circuits (I^2C) – PC Parallel port programming -ISA/PCI Bus protocols – Firewire

UNIT - II USB AND CAN BUS 10

USB bus – Introduction – Speed Identification on the bus – USB States – USB bus communication: Packets –Data flow types –Enumeration –Descriptors –PIC 18 Microcontroller USB Interface – C Programs –CAN Bus – Introduction - Frames –Bit stuffing –Types of errors –Nominal Bit Timing – PIC microcontroller CAN Interface –A simple application with CAN

UNIT - III ETHERNET BASICS 9

Elements of a network – Inside Ethernet – Building a Network: Hardware options – Cables, Connections and network speed – Design choices: Selecting components – Ethernet Controllers – Using the internet in local and internet communications – Inside the Internet protocol

UNIT - IV EMBEDDED ETHERNET 9

Exchanging messages using UDP and TCP – Serving web pages with Dynamic Data – Serving web pages that respond to user Input – Email for Embedded Systems – Using FTP – Keeping Devices and Network secure.

UNIT - V WIRELESS EMBEDDED NETWORKING 9

Wireless sensor networks – Introduction – Applications – Network Topology – Localization –Time Synchronization - Energy efficient MAC protocols –SMAC – Energy efficient and robust routing – Data Centric routing

L = 45 T = 15 TOTAL = 60 PERIODS

TEXT BOOKS

1. Frank Vahid, Givargis ‘Embedded Systems Design: A Unified Hardware/Software Introduction’, Wiley Publications
2. Jan Axelson, ‘Parallel Port Complete’ , Penram publications
3. Dogan Ibrahim, ‘Advanced PIC microcontroller projects in C’, Elsevier 2008
4. Jan Axelson ‘Embedded Ethernet and Internet Complete’, Penram publications
5. Bhaskar Krishnamachari, ‘Networking wireless sensors’, Cambridge press 2005

SY9324 **EMBEDDED SYSTEM LAB II** **L T P C**
0 0 3 2

LIST OF EXPERIMENTS

1 Embedded DSP based System Designing.
   (a) Analog DSP tool kit.
   (b) Code compressor studio for embedded DSP using Texas tool kit.
2 IPCORE usage in VOIP Through SoC2 tools
   (a) Cypress PsoC designing Tools
   (b) SoPC designing Tools
3 ARM - Assembly Language Programming
4 Programming with DSP processors for Correlation, Convolution, Arithmetic adder, Multiplier, Design of Filters – FIR based , IIR based
5. Design with Programmable Logic Devices using Xilinx/Altera FPGA and CPLD
   Design and Implementation of simple Combinational/Sequential Circuits
6. Network Simulators
   Simple wired/ wireless network simulation using NS2

TOTAL :45 PERIODS

SY9351 **DATA COMMUNICATION & NETWORKS** **L T P C**
3 0 0 3

UNIT – I INTRODUCTION **9**

Components of network – Topologies – WAN / LAN – OSI – ISO layered Architecture Modulation and demodulation – Bit error rates – Line coding – Error correcting codes.

UNIT - II DATA LINK LAYER **9**

Design issues – CRC technique and sliding window techniques – Performance analysis of sliding window techniques – Framing formats – Case Study – HDLC protocols – Medium access control – CSMA / CD – Token ring and token bus – FDDI – Wireless LAN – Performance analysis of MAC protocols – Bridges.

UNIT - III NETWORK LAYER **9**

Circuit switching – packet switching – Design issues – IP addressing and IP diagram – Routers and gateways – Routing –Sub netting – CIDR – ICMP – ARP – RARP – Ipv6 – QoS.

UNIT – IV TRANSPORT LAYER **9**

TCP and UDP – Error handling and flow control – Congestion control – TCP Retransmission – Timeout – Socket Abstraction.

UNIT – V APPLICATION SERVICES 9

Simple Mail Transfer Protocol (SMTP) – File Transfer Protocols (FTP), telnet, the World Wide Web (WWW), Hypertext Transfer Protocol (HTTP), Domain name service (DNS), Security, Multimedia applications.

TOTAL : 45 PERIODS

REFERENCES:

1. William Stallings, “Data and Computer Communications”, Seventh Edition, Prentice Hall, 2003.
2. Larry Peterson, Bruce S Davie “Computer Networks: A Systems Approach”, Morgan Kaufmann Publishers, 2nd Edition, 1999
3. James F Kurose, “Computer Networking: A Top – Down Approach Featuring the Internet”, Addison Wesley, 2nd Edition 2002.
4. W.Richard Stevens and Gary R Wright, “TCP / IP Illustrated”, Addison Wesley, Volume 1 & 2, 2001.
5. Douglas E Corner, “Internetworking with TCP / IP”, Volume 1 & 2, 2000.

SY9352	DIGITAL IMAGE PROCESSING	L	T	P	C
		3	0	0	3

UNIT – I DIGITAL IMAGE FUNDAMENTALS 9

Elements of digital image processing systems, Elements of visual perception, psycho visual model, brightness, contrast, hue, saturation, mach band effect, Color image fundamentals - RGB,HSI models, Image acquisition and sampling, Quantization, Image file formats, Two-dimensional convolution, correlation, and frequency responses.

UNIT – II IMAGE TRANSFORMS 9

1D DFT, 2D transforms – DFT, DCT, Discrete Sine, Walsh, Hadamard, Slant, Haar, KLT, SVD, Radon, and Wavelet Transform.

UNIT – III IMAGE ENHANCEMENT AND RESTORATION 9

Histogram modification and specification techniques, Noise distributions, Spatial averaging, Directional Smoothing, Median, Geometric mean, Harmonic mean, Contra harmonic filters, Homomorphic filtering, Color image enhancement. Image Restoration – degradation model, Unconstrained and Constrained restoration, Inverse filtering, Wiener filtering, Geometric transformations– spatial transformations, Gray-Level interpolation,

UNIT – IV IMAGE SEGMENTATION AND RECOGNITION 9

Edge detection. Image segmentation by region growing, region splitting and merging, edge linking, Morphological operators: dilation, erosion, opening, and closing. Image Recognition– Patterns and pattern classes, matching by minimum distance classifier, Statistical Classifier. Matching by correlation, Neural network application for image recognition.

UNIT – V IMAGE COMPRESSION 9

Need for image compression, Huffman, Run Length Encoding, Arithmetic coding, Vector Quantization, Block Truncation Coding. Transform Coding – DCT and Wavelet. Image compression standards.

TOTAL :45 PERIODS

REFERENCES:

1. Rafael C. Gonzalez, Richard E.Woods, 'Digital Image Processing', Pearson Education, Inc., Second Edition, 2004.
2. Anil K.Jain,'Fundamentals of Digital Image Processing',Prentice Hall of India,02.
3. David Salomon : Data Compression – The Complete Reference, Springer Verlag New York Inc., 2nd Edition, 2001
4. Rafael C. Gonzalez, Richard E.Woods, Steven Eddins, ' Digital Image Processing using MATLAB', Pearson Education, Inc., 2004.
5. William K.Pratt, ' Digital Image Processing', John Wiley, NewYork, 2002.
6. Milman Sonka, Vaclav Hlavac, Roger Boyle, 'Image Processing, Analysis, and Machine Vision', Brooks/Cole, Vikas Publishing House, II ed., 1999.
7. Sid Ahmed, M.A., 'Image Processing Theory, Algorithms and Architectures', McGrawHill, 1995.
8. Lim, J.S., 'Two Dimensional Signal and Image Processing', Prentice-Hall, New Jersey, 1990.

SY9353 ASIC DESIGN L T P C
3 0 0 3

UNIT – I INTRODUCTION TO ASICS, CMOS LOGIC AND ASIC LIBRARY DESIGN 9

Types of ASICs – Design Flow – CMOS transistors, CMOS design rules – Combinational Logic Cell – Sequential logic cell – Data path logic cell – Transistors as Resistors – Transistor Parasitic Capacitance – Logical effort – Library cell design – Library architecture.

UNIT - II PROGRAMMABLE ASICS, PROGRAMMABLE ASIC LOGIC CELLS AND PROGRAMMBALE ASIC I/O CELLS 9

Anti fuse – static RAM – EPROM and EEPROM technology – PREP bench marks – Actel ACT – Xilinx LCA – Altera FLEX – Altera MAX DC & AC inputs and outputs – Clock and power inputs – Xilinx I/O blocks.

UNIT – III PROGRAMMABLE ASIC INTERCONNECT, PROGRAMMABLE ASIC DESIGN SOFTWARE AND LOW LEVEL DESIGN ENTRY. 9

Actel ACT – Xilinx LCA – Xilinx EPLD – Altera MAX 5000 and 7000 – Altera MAX 9000 Altera FLEX – Design systems – Logic Synthesis – Half Gate ASIC – Schematic entry – Low level design language – PLA tools – EDIF – CFI design representation.

UNIT – IV LOGIC SYNTHESIS, SIMULATION AND TESTING 9

Verilog and logic synthesis – VHDL and logic synthesis - Types of simulation – Boundary scan test – Fault simulation – Automatic test pattern generation.

UNIT – V ASIC CONSTRUCTION, FLOOR PLANNING, PLACEMENT AND ROUTING 9

System partition – FPGA partitioning – partitioning methods – floor planning – placement – physical design flow – global routing – detailed routing – special routing – circuit extraction – DRC.

TOTAL : 45 PERIODS

REFERENCES:

1. M.J.S. SMITH, “Application – Specific Integrated Circuits” – Addison – Wesley Longman Inc., 1997.
2. Andrew Brown, “VLSI Circuits and Systems in Silicon”, McGraw Hill, 1991.
3. S.D.Brown, R.J.Francis, J.Rox, Z.G.Uranesic, “Field Programmable Gate Arrays” – Kluever Academic Publishers, 1992.
4. Mohammed Ismail and Terri Fiez, “Analog VLSI Signal and Information Processing”, McGraw Hill, 1994.
5. S.Y. Kung, H.J.Whilo House, T.Kailath, “VLSI and Modern Signal Processing”, Prentice Hall, 1985.
6. Jose E.France, Yannis Tsividis, “Design of Analog – Digital VLSI Circuits for Telecommunication and Signal Processing”, Prentice Hall, 1994.

SY9354 ADVANCED EMBEDDED SYSTEMS

L	T	P	C
3	0	0	3

UNIT – I INTRODUCTION AND REVIEW OF EMBEDDED HARDWARE 9

Terminology – Gates – Timing diagram – Memory – Microprocessor buses – Direct memory access – Interrupts – Built interrupts – Interrupts basis – Shared data problems – Interrupt latency - Embedded system evolution trends – Round-Robin – Round Robin with interrupt function – Rescheduling architecture – algorithm.

UNIT - II REAL TIME OPERATING SYSTEM 9

Task and Task states – Task and data – Semaphore and shared data operating system services – Message queues timing functions – Events – Memory management – Interrupt routines in an RTOS environment – Basic design using RTOS.

UNIT – III EMBEDDED HARDWARE, SOFTWARE AND PERIPHERALS 9

Custom single purpose processors: Hardware – Combination Sequence – Processor design – RT level design – optimising software: Basic Architecture – Operation – Programmers view – Development Environment – ASIP – Processor Design – Peripherals – Timers, counters and watch dog timers – UART – Pulse width modulator – LCD controllers – Key pad controllers – Stepper motor controllers – A/D converters – Real time clock.

UNIT – IV MEMORY AND INTERFACING 9

Memory: Memory write ability and storage performance – Memory types – composing memory – Advance RAM interfacing communication basic – Microprocessor interfacing I/O addressing – Interrupts – Direct memory access – Arbitration multilevel bus architecture – Serial protocol – Parallel protocols – Wireless protocols – Digital camera example.

UNIT – V CONCURRENT PROCESS MODELS AND HARDWARE SOFTWARE CO-DESIGN 9

Modes of operation – Finite state machines – Models – HCFSL and state charts language – state machine models – Concurrent process model – Concurrent process – Communication among process –Synchronization among process – Implementation – Data Flow model. Design technology; Automation synthesis – Hardware software co-simulation – IP cores – Design Process Model.

TOTAL : 45 PERIODS

REFERENCES:

1. David. E.Simon “An Embedded Software Primer”, Pearson Education, 2001.
2. Frank Vahid and Tony Gwargie “Embedded System Design”, John Wiley & sons, 2002.
3. Steve Heath, “Embedded System Design”, Elserien, Second Edition, 2004.

SY9355	COMPUTER ARCHITECTURE	L	T	P	C
		3	0	0	3

UNIT – I FUNDAMENTALS OF COMPUTER DESIGN 9

Review of fundamentals of CPU, Memory and IO – Performance evaluation – Instruction set principles – Design issues – Example Architectures.

UNIT – II INSTRUCTION LEVEL PARALLELISM 9

Pipelining and handling hazards – Dynamic Scheduling – Dynamic hardware prediction – Multiple issue – Hardware based speculation – Limitations of ILP – Case studies.

UNIT - III INSTRUCTION LEVEL PARALLELISM WITH SOFTWARE APPROACHES **9**

Compiler techniques for exposing ILP – Static branch prediction – VLIW & EPIC – Advanced compiler support – Hardware support for exposing parallelism – Hardware versus software speculation mechanisms – IA 64 and ltanium processor.

UNIT – IV MEMORY AND I/O **9**

Cache performance – Reducing cache miss penalty and miss rate – Reducing hit time – Main memory and performance – Memory technology. Types of storage devices – Buses – RAID – Reliability, availability and dependability – I/O performance measures – Designing an I/O system.

UNIT – V MULTIPROCESSORS AND THREAD LEVEL PARALLELISM **9**

Symmetric and distributed shared memory architectures – Performance issues – Synchronization – Models of memory consistency – Multithreading.

TOTAL: 45 PERIODS

REFERENCES:

1. John L.Hennessey and David A.Patterson, “Computer Architecture: A Quantitative Approach”, Third Edition, Morgan Kaufmann, 2003.
2. D.Sia, T.Fountain and P.Kacsuk, “Advanced computer Architectures: A Design Space Approach”, Addion Wesley, 2000.

SY9356 MULTIMEDIA SYSTEMS

L	T	P	C
3	0	0	3

UNIT - I MULTIMEDIA **9**

Introduction – Multimedia modalities, Channels and Medium – Interaction – Communicative Interaction – Objects and Agents – Channels of Communication – Artificial Languages – Natural Communication – Meta-languages – Components of Interactive Multimedia Systems.

UNIT - II KNOWLEDGE AND USER UNDERSTANDING **9**

Knowledge – Basic idea of knowledge – A working definition – Knowledge representation – Knowledge Elicitation – Know about user applying user knowledge – acquiring user knowledge – User profiling – User modelling.

UNIT – III INTERACTION, INTERFACE & SEMIOTICS **9**

Traditional HCI – Modalities and the interface – Interface channels – Functionality and usability – Visual appearance and Graphic design – Multimedia content – Semiotics – Idea of a Sign – Comples Signs – Semiotics and Media.

UNIT - IV TEXT AND SOUND **9**

Visual Perception of Text – Images on Page – Meaning and Text Readability – Text and the Screen – Modality of Sound – Channels of Communication – Combining Sound Chanles – Technology of Sound – MIDI

UNIT – V IMAGES **9**

Psychology of vision – Representational Images – Juxtaposition of Images – Perception of Motion – Constructing a Shot – Shots into narrative – Modern languages of film and television.

TOTAL: 45 PERIODS

REFERENCES:

1. Mark Elsom-Cook, “Principles of Interactive Multimedia” McGraw Hill, International Edition 2001.

SY9357 OPERATING SYSTEMS

L	T	P	C
3	0	0	3

UNIT - I **9**

Introduction – Operating systems and services – Processes – CPU Scheduling approaches.

UNIT - II **9**

Process synchronization – Semaphores – Deadlocks – Handling deadlocks – Multithreading.

UNIT - III **9**

Memory management – Paging – Segmentation – Virtual memory – Demand paging – Replacement algorithms.

UNIT - IV **9**

Disk Scheduling approaches – File systems – Design issues – User interfaces to file systems – I / O device management.

UNIT - V **9**

Case study – Design and implementation of the UNIX OS, process model and Structure – Memory management – File system – UNIX I / O management and Device drivers – Windows – System components – Process management – Memory management – File systems – Networking.

TOTAL: 45 PERIODS

REFERENCES:

1. Abraham Silberschatz Peter B. Galvin, G.Gagne, “Operating System Concepts”, 6th Edition, Wesley Publishing company, 2003.
2. M.J.Bach, Design of the UNIX Operating System, Prentice Hall, 1986.

SY9358	VHDL	L	T	P	C
		3	0	0	3

UNIT - I VHDL FUNDAMENTALS **9**

Fundamental Concepts – Modeling Digital Systems – Domains and Levels of Modeling – Modeling Languages – VHDL Modeling concepts – Scalar Data Types and Operations – Constants and variables – Scalar Types – Type Classification – Attributes and Scalar types – Expressions and operators – Sequential Statements – If statements – Case statements – Null Statements – Loop statements – Assertion and Report statements.

UNIT – II COMPOSITE DATA TYPES & BASIC MODELING CONSTRUCTS **9**

Arrays – Unconstrained Array types – Array Operations and Referencing – Records – Basic Modeling Constructs – Entity Declarations – Architecture Bodies – Behavioral Descriptions – Structural Descriptions – Design Processing. Case Study: A pipelined Multiplier Accumulator.

UNIT - III SUBPROGRAMS AND PACKAGES **9**

Procedures – Procedure Parameters – Concurrent Procedure Call Statements – functions – Overloading – Visibility of Declarations – Packages and Use Clauses – Package declarations – Package bodies – Use Clauses – The predefined – Aliases - Aliases for data objects – Aliases for Non-Data Items. Case Study: A Bit-Vector Arithmetic Package.

UNIT – IV SIGNALS, COMPONENTS, CONFIGURATIONS **9**

Basic Resolved signals – IEEE Std_Logic_1164 Resolved subtypes – Resolved signal parameters – Generic Constants – Parameterizing behavior – Parameterizing structure – Components and Configurations – Components – Configuring component Instances – Configuration Specification – Generate Statements – generating iterative structure –

Conditionally generating structures – Configuration of generate Statements. Case Study: The DLX Computer System.

UNIT – V ADTs AND FILES 9

Access Types – Linked Data structures – Abstract Data Types using Packages – Files and Input/Output – Files – The Package Textio – Verilog. Case Study: Queuing Networks.

TOTAL: 45 PERIODS

REFERENCES:

1. Peter J.Ashenden, The Designer's Guide to VHDL, Morgan Kaufmann Publishers, San Francisco, Second Edition, May 2001.
2. Zainalabedin Navabi, VHDL Analysis and Modeling of Digital Systems, McGraw Hill International Editions, Second Edition, 1998.
3. James M.Lee, Verilog Quick start, Kluwer Academic Publishers, Second Edition, 1999.

SY9359	ADVANCED MICROPROCESSORS AND MICRO CONTROLLERS DESIGN	L	T	P	C
		3	0	0	3

UNIT - I MICROPROCESSOR ARCHITECTURE 9

Instruction set – Data formats – Instruction formats – Addressing modes – Memory hierarchy – register file – Cache – Virtual memory and paging – Segmentation – Pipelining – The instruction pipeline – pipeline hazards – Instruction level parallelism – reduced instruction set – Computer principles – RISC versus CISC – RISC properties – RISC evaluation – On-chip register files versus cache evaluation

UNIT - II HIGH PERFORMANCE CISC ARCHITECTURE – PENTIUM 9

The software model – functional description – CPU pin descriptions – RISC concepts – bus operations – Super scalar architecture – pipe lining – Branch prediction – The instruction and caches – Floating point unit –protected mode operation – Segmentation – paging – Protection – multitasking – Exception and interrupts – Input /Output – Virtual 8086 model – Interrupt processing -Instruction types – Addressing modes – Processor flags – Instruction set - programming the Pentium processor.

UNIT - III HIGH PERFORMANCE RISC ARCHITECTURE : ARM 9

The ARM architecture – ARM assembly language program – ARM organization and implementation – The ARM instruction set - The thumb instruction set – ARM CPU cores.

UNIT - IV MOTOROLA 68HC11 MICROCONTROLLERS 9

Instructions and addressing modes – operating modes – Hardware reset – Interrupt system – Parallel I/O ports – Flags – Real time clock – Programmable timer – pulse accumulator – serial communication interface – A/D converter – hardware expansion – Assembly language Programming

UNIT - V PIC MICRO CONTROLLER 9

CPU architecture – Instruction set - Interrupts – Timers – I/O port expansion –I^2C bus for peripheral chip access – A/D converter – UART

TOTAL: 45 PERIODS

REFERENCES:

1. Daniel Tabak , '' Advanced Microprocessors" McGraw Hill.Inc., 1995
2. James L. Antonakos, "The Pentium Microprocessor '' Pearson Education, 1997.
3. Steve Furber, '' ARM System –On –Chip architecture "Addison Wesley, 2000.
4. Gene .H.Miller." Micro Computer Engineering," Pearson Education, 2003.
5. John .B.Peatman, "Design with PIC Microcontroller, Prentice hall, 1997.
6. James L.Antonakos," An Introduction to the Intel family of Microprocessors '' Pearson Education 1999.
7. Barry.B.Breg," The Intel Microprocessors Architecture , Programming and Interfacing ", PHI, 2002.
8. Valvano "Embedded Microcomputer Systems" Thomson Asia PVT LTD first reprint 2001

Readings :

Web links

www.ocw.nit.edu

www.arm.com

SY9360 DSP INTEGRATED CIRCUITS L T P C
3 0 0 3

UNIT - I DSP INTEGRATED CIRCUITS AND VLSI CIRCUIT TECHNOLOGIES 9

Standard digital signal processors, Application specific IC's for DSP, DSP systems, DSP system design, Integrated circuit design. MOS transistors, MOS logic, VLSI process technologies, Trends in CMOS technologies.

UNIT - II DIGITAL SIGNAL PROCESSING 9

Digital signal processing, Sampling of analog signals, Selection of sample frequency, Signal-processing systems, Frequency response, Transfer functions, Signal flow graphs, Filter structures, Adaptive DSP algorithms, DFT-The Discrete Fourier Transform, FFT-The Fast Fourier Transform Algorithm, Image coding, Discrete cosine transforms.

UNIT - III DIGITAL FILTERS AND FINITE WORD LENGTH EFFECTS 9

FIR filters, FIR filter structures, FIR chips, IIR filters, Specifications of IIR filters, Mapping of analog transfer functions, Mapping of analog filter structures, Multirate systems, Interpolation with an integer factor L, Sampling rate change with a ratio L/M, Multirate filters. Finite word length effects -Parasitic oscillations, Scaling of signal levels, Round-off noise, Measuring round-off noise, Coefficient sensitivity, Sensitivity and noise.

UNIT - IV DSP ARCHITECTURES AND SYNTHESIS OF DSP ARCHITECTURES 9

DSP system architectures, Standard DSP architecture, Ideal DSP architectures, Multiprocessors and multicomputers, Systolic and Wave front arrays, Shared memory

architectures. Mapping of DSP algorithms onto hardware, Implementation based on complex PEs, Shared memory architecture with Bit – serial PEs.

UNIT - V ARITHMETIC UNITS AND INTEGRATED CIRCUIT DESIGN 9

Conventional number system, Redundant Number system, Residue Number System. Bit-parallel and Bit-Serial arithmetic, Basic shift accumulator, Reducing the memory size, Complex multipliers, Improved shift-accumulator. Layout of VLSI circuits, FFT processor, DCT processor and Interpolator as case studies.

L:45 TOTAL :45 PERIODS

REFERENCES:

1. Lars Wanhammer, “DSP Integrated Circuits”, 1999 Academic press, New York.
2. A.V.Oppenheim et.al, ‘Discrete-time Signal Processing’ Pearson education, 2000.
3. Emmanuel C. Ifeachor, Barrie W. Jervis, “ Digital signal processing – A practical approach”, Second edition, Pearson edition, Asia.
4. 4.Keshab K.Parhi, ‘VLSI digital Signal Processing Systems design and Implementation’ John Wiley & Sons, 1999.

SY9361	EMBEDDED ANALOG INTERFACING	L	T	P	C
		3	0	0	3

UNIT - I MEASUREMENT SYSTEM DESIGN 9

Characteristics of Instrumentation – Measurement accuracy – Measurement standards - Dynamic Range – Calibration – Bandwidth – Digital interfacing advantages

UNIT - I ANALOG-TO-DIGITAL CONVERTERS 9

Types of ADCs - ADC Comparison - Sample and Hold - ADC Types - Flash ADC - Successive Approximation ADC - Dual-Slope (Integrating) ADC - Sigma-Delta ADC - Microprocessor Interfacing - Clocked Interfaces - Serial Interfaces – Integrated ADC Embedded Controllers

UNIT - III SENSORS & PERIPHERALS 9

Temperature Sensors - Optical Sensors – CCDs - Magnetic Sensors - Motion/Acceleration Sensors - Strain Gauges - Solenoids – Heaters – Coolers – LEDs – DACs - Digital Potentiometers - Analog Switches - Stepper Motors - DC Motors

UNIT - IV OUTPUT CONTROL METHODS 9

Measuring Period versus Frequency - Voltage-to-Frequency Converters - Open-Loop Control - Negative Feedback and Control - Microprocessor-Based Systems- On-Off Control - Proportional Control - Proportional, Integral, Derivative Control - Motor Control - Predictive Control - Measuring and Analyzing Control Loops

UNIT - V MICROCONTROLLER INTERFACING 9

Standard Interfaces - IEEE 1451.2 - 4–20 ma Current Loop – Fieldbus - Microcontroller Supply and Reference - Resistor Networks - Multiple Input Control -AC Control - Voltage Monitors and Supervisory Circuits - Driving Bipolar Transistors/ MOSFET- Reading Negative Voltages – PWM based control

TOTAL: 45 PERIODS

REFERENCES:

1. Stuart R. Ball, Analog Interfacing to Embedded Microprocessor Systems, Newnes, 2nd Edition ,2003.
2. John G. Webster , Handbook of measurement, Instrumentation, & sensors, John Wiley & Sons Inc, New York-1998.
3. Dogan Ibrahim, Microcontroller-Based Temperature Monitoring and Control, Newnes, 2nd Edition ,2002.

SY9362 EMBEDDED AUTOMOTIVE NETWORKING WITH CAN

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UNIT - I DATA COMMUNICATION BASICS 9

Data communication basics - Network communication protocol – Medium access control – Error checking & control – Requirements & applications of field bus systems- Characteristics of CAN

UNIT - II CAN DATA LINK LAYER 9

CAN data link layer – Principles of bus arbitration – Frame formats – Error detection & error handling – Extended frame format – Time triggered multiplexing

UNIT - III CAN PHYSICAL LAYER 9

Physical signaling – Transmission media – Network topology – Bus medium access – Physical layer standards -

UNIT - IV CAN PROTOCOL CONTROLLERS 9

CAN protocol controllers – Functions of a CAN controller – Message filtering – Message handling - Standalone CAN controllers – Integrated CAN controllers – CAN transceivers

UNIT - V CAN HIGHER LAYER PROTOCOLS 9

CAN application layer – Protocol architecture – CAN message specification – Allocation of message identifiers – Network management – Layer management – Higher layer protocols - CAN open - DeviceNet – SAEJ1939 – Time triggered CAN

TOTAL: 45 PERIODS

REFERENCES:

1. Konrad Etschberger, Controller Area Network , IXXAT Automation GmbH,2001
2. Wolfhard Lawrenz, CAN System Engineering: From Theory to Practical Applications, Springer,1997.
3. Glaf P.Feiffer, Andrew Ayre and Christian Keyold “Embedded Networking with CAN and CAN open”. Embedded System Academy 2005.
4. Francoise Simonot-Lion, Handbook of Automotive Embedded Systems ,CRC Press,2007.
5. http://www.can-cia.org/can/
6. http://www.semiconductors.bosch.de/en/20/can/3-literature.asp

SY9363	REAL TIME SYSTEMS	L	T	P	C
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UNIT I INTRODUCTION 9

Introduction – Issues in Real Time Computing, Structure of a Real Time System, Task classes, Performance Measures for Real Time Systems, Estimating Program Run Times. Task Assignment and Scheduling – Classical uniprocessor scheduling algorithms, Uniprocessor scheduling of IRIS tasks, Task assignment, Mode changes, and Fault Tolerant Scheduling.

UNIT II PROGRAMMING LANGUAGES AND TOOLS 9

Programming Languages and Tools – Desired language characteristics, Data typing, Control structures, Facilitating Hierarchical Decomposition, Packages, Run – time (Exception) Error handling, Overloading and Generics, Multitasking, Low level programming, Task Scheduling, Timing Specifications, Programming Environments, Run – time support**.**

UNIT III REAL TIME DATABASES 9

Real time Databases – Basic Definition, Real time Vs General Purpose Databases, Main Memory Databases, Transaction priorities, Transaction Aborts, Concurrency control issues, Disk Scheduling Algorithms, Two – phase Approach to improve Predictability, Maintaining Serialization Consistency, Databases for Hard Real Time Systems.

UNIT IV COMMUNICATION 9

Real – Time Communication – Communications media, Network Topologies Protocols, Fault Tolerant Routing. Fault Tolerance Techniques – Fault Types, Fault Detection. Fault Error containment Redundancy, Data Diversity, Reversal Checks, Integrated Failure handling.

UNIT V EVALUATION TECHNIQUES 9

Reliability Evaluation Techniques – Obtaining parameter values, Reliability models for Hardware Redundancy, Software error models. Clock Synchronization – Clock, A Nonfault – Tolerant

Synchronization Algorithm, Impact of faults, Fault Tolerant Synchronization in Hardware, Fault Tolerant Synchronization in software.

L:45 TOTAL: 45 PERIODS

REFERENCES:

1. C.M. Krishna, Kang G. Shin, "Real – Time Systems", McGraw – Hill International Editions, 1997.
2. Stuart Bennett, "Real Time Computer Control – An Introduction", Prentice Hall of India, 1998.
3. Peter D.Lawrence, "Real Time Micro Computer System Design – An Introduction", McGraw Hill, 1988.
4. S.T. Allworth and R.N.Zobel, "Introduction to real time software design", Macmillan, 2nd Edition, 1987.
5. R.J.A Buhur, D.L Bailey, "An Introduction to Real – Time Systems", Prentice – Hall International, 1999.
6. Philip.A.Laplante, "Real Time System Design and Analysis", Prentice Hall of India, 3rd Edition, April 2004.

SY9364 REAL TIME EMBEDDED OPERATING SYSTEM

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UNIT – I INTRODUCTION TO EMBEDDED SYSTEM 9

Introduction - Embedded systems description, definition, design considerations & requirements - Overview of Embedded system Architecture (CISC and RISC) - Categories of Embedded Systems - embedded processor selection &tradeoffs - Embedded design life cycle - Product specifications - hardware/software partitioning - iterations and implementation - hardware software integration - product testing techniques – ARM 7

UNIT – II OPERATING SYSTEM OVERVIEW 9

Introduction –Advantage and Disadvantage of Using RTOS – Multitasking – Tasks - Real Time Kernels – Scheduler - Non-preemptive Kernels - Preemptive Kernels – Reentrancy- Reentrant Functions – Round Robin Scheduling - Task Priorities - Static Priorities – Mutual Exclusion – Deadlock – Intertask Communication – Message Mailboxes – Message Queues - Interrupts - Task Management – Memory Management -Time Management – Clock Ticks.

UNIT - III 9

Introduction - µC/OS-II Features - Goals of µC/OS-II - Hardware and Software Architecture – Kernel Structures: Tasks –Task States – Task Scheduling – Idle Task – Statistics Task – Interrupts Under µC/OS-II – Clock Tick - µC/OS-II Initialisation. Task Management: Creating Tasks – Task Stacks – Stack Checking – Task's Priority – Suspending Task – Resuming Task. Time Management: Delaying a Task Resuming a Delayed Task – System Time. Event Control Blocks- Placing a Task in the ECB Wait List – Removing a Task from an ECB wait List .

UNIT - IV **9**

Semaphore Management: Semaphore Management Overview – Signaling a Semaphore.Message Mailbox Management: Creating a Mailbox – Deleting Mailbox – Waiting for a Message box – Sending Message to a Mailbox- Status of Mailbox . Message Queue Management: Creating Message Queue – Deleting a Message Queue – Waiting for a Message at a Queue – Sending Message to a Queue – Flushing a Queue.

UNIT - V **9**

Memory Management: Memory Control Blocks – Creating Partition- Obtaining a Memory Block – Returning a Memory Block .Getting Started with µC/OS-II – Installing µC/OS-II – Porting µC/OS-II: Development Tools – Directories and Files – Testing a Port - IAR Workbench with µC/OS-II - µC/OS-II Porting on a 8051 CPU – Implementation of Multitasking - Implementation of Scheduling and Rescheduling – Analyze the Multichannel ADC with help of µC/OS-II.

TOTAL: 60 PERIODS

REFERENCES:

1. Jean J. Labrosse, MicroC/OS – II The Real Time Kernel, CMP Books, 2nd Edition 1998.
2. David Seal, ARM Architecture Reference Manual, 2005.
3. Steve Furbe, ARM System-on-Chip Architecture, Addison-Wesley Professional, 2 edition 2000.

SY9365	VLSI ARCHITECTURE AND DESIGN METHODOLOGIES	L	T	P	C
		3	0	0	3

UNIT I INTRODUCTION **9**

Overview of digital VLSI design methodologies – Trends in IC Technology – Advanced Boolean algebra – Shannon's expansion theorem – Consensus theorem – Octal designation- Run measure – Buffer gates - Gate expander – Reed Muller expansion – Synthesis of multiple output combinational logic circuits by product map method – Design of static hazard free, dynamic hazard free logic circuits.

UNIT II ANALOG VLSI AND HIGH SPEED VLSI **9**

Introduction to analog VLSI – realization of neural networks and switched capacitor filters – Sub-micron technology and Gas VLSI Technology.

UNIT III PROGRAMMABLE ASICS **9**

Anti fuse – static RAM – EPROM and technology – PREP bench marks – Actel ACT – Xilinx LCA – Altera flex – Altera MAX DC & AC inputs and outputs – Clock and power inputs – Xilinx I/O blocks.

UNIT IV PROGRAMMABLE ASIC DESIGN SOFTWARE 9

Actel ACT – Xilinux LCA – Xilinux EPLD – Altera MAX 5000 and 7000 – Altera MAX 9000 – design systems – logic synthesis – half gate – schematic entry – Low level design language – PLA tools – EDIF – CFI design representation.

UNIT V LOGIC SYNTHESIS, SIMULATION AND TESTING 9

Basic features of VHDL language for behavioral modeling and simulation – Summary of VHDL data types – Dataflow and structural modeling – VHDL and logic synthesis – Circuit and layout verification – Types of simulation – Boundary scan test – Fault simulation – Automatic test pattern generation – design examples.

TOTAL: 45 PERIODS

REFERENCES:

1. William I. Fletcher, “An Engineering Approach to Digital Design”, Prentice Hall of India.
2. Amar Mukharjee, “Introduction to NMOS and CMOS VLSI System Design”, Prentice Hall, 1986.
3. M.J.S. Smith, “Application – specific integrates circuits”, Addison Wesley Longman Inc. 1997.
4. Frederick J.Hill and Gerald R.Peterson, “Computer Aided Logical Design with emphasis on VLSI”.

SY9366	EMBEDDED SYSTEM DESIGN USING ARM PROCESSOR	L	T	P	C
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UNIT – I PRINCIPLES OF EMBEDDED SYSTEM 9

Introduction - Embedded systems description, definition, design considerations & requirements - Overview of Embedded system Architecture - Categories of Embedded Systems - Product specifications - hardware/software partitioning - iterations and implementation - hardware software integration - product testing techniques. Wired Communication Protocols: UART - Inter Integrated Circuit (I2C) - Serial Peripheral Interface (SPI) - Controller Area Network (CAN).Wireless communication Protocols: Zigbee Protocols – Blue tooth Protocols - IrDA.

UNIT – II ARM PROCESSOR FUNDAMENTALS 9

ARM core Introduction – Registers – Current Program Status Register – Pipeline – Exception – Interrupts – Vector Table – Core Extension – Architecture Revisions – ARM Processor Families – ARM Instruction Set – Thumb Instruction set – Thumb Register Usuage – ARM – Thumb Interworking – Stack Instruction – Software Interrupt Instruction.

UNIT - III CACHES AND MMU 9

The Memory Hierarchy and Cache Memory – Cache Architecture - Cache Policy – Co Processor and Caches – Flushing and Cleaning Cache Memory – Cache Lockdown – Caches and Software Performance. MMU: Moving from an MPU to an MMU – Virtual Memory – Details of ARM MMU – The Caches and Write Buffer – Co Processor and MMU configuration.

UNIT – IV OPTIMIZED PRIMITIVES 9

Double Precision Integer Multiplication – Integer Normalization and count Leading Zeros – Division – Square Roots – Transcendental Functions : Log,,exp,sin,cos – Endian Reversal and Bit Operations – Saturated and Rounded Arithmetic – Random Number Generation

UNIT – V WRITING AND OPTIMIZING ARM ASSEMBLY CODE 9

Writing Assembly Code – Profiling and Cycle Counting – Instruction Scheduling – Register Allocation – Conditional Execution – Looping Constructs – Bit Manipulation – Efficient Switches – Handling Unaligned Data.

TOTAL :45 PERIODS

REFERENCES:

1. Andrew N.Sloss, Dominic Symes, Chris Wright, “ARM System Developer’s Guide”, Morgan Kaufmann Series in Computer Architecture and Design, 2004.
2. Tammy Noergaard, “Embedded Systems Architecture”, Newnes, 2005.
3. David Seal, “ARM Architecture Reference Manual”, 2005.
4. Steve Furbe, “ARM System-on-Chip Architecture”, Addison-Wesley Professional, 2nd Edition, 2000.